In the Claims

Please cancel Claim 19. The claims currently pending in the application are as follows:

1. (previously presented) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

interleaved clock generator means of a first type for receiving the input clock signal and for generating in response thereto *M* interleaved intermediate clock signals, where *M* is a factor of *N* and is an integer greater than unity, the interleaved clock generator means of the first type including one of (a) a multi-stage serial-delay circuit and (b) a ring counter circuit; and

M interleaved clock generator means of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator means of the first type and for generating in response thereto N/M of the *N* interleaved clock signals, each of the interleaved clock generator means of the second type including the other of (a) the multi-stage serial-delay circuit and (b) the ring counter circuit, wherein:

corresponding edges of temporally adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N*Td);

the input clock signal has a frequency of 1/(M*Td) when the interleaved clock generator means of the first type includes the multi-stage serial delay circuit; and

the input clock signal has a frequency of M/(N*Td) when the interleaved clock generator means of the first type includes the ring counter circuit.

2. (original) The interleaved clock generator of claim 1, in which the multi-stage serial-delay circuit includes a delay-locked loop.

3. (original) The interleaved clock generator of claim 1, in which the multi-stage serial-delay circuit includes a phase-locked loop.

4. (cancel)

5. (original) The interleaved clock generator of claim 1, in which:

the interleaved clock generator means of the first type includes the multi-stage serial-delay circuit; and

each of the interleaved clock signal generator means of the second type includes the ring counter circuit.

6. (original) The interleaved clock generator of claim 5, in which the ring counter circuit includes an N/M-stage ring counter.

7. (original) The interleaved clock generator of claim 5, in which the multi-stage serial-delay circuit includes *M* delay stages, each providing one of the intermediate clock signals.

8. (previously presented) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

interleaved clock generator means of a first type for receiving the input clock signal and for generating in response thereto *M* interleaved intermediate clock signals, where *M* is a factor of *N* and is an integer greater than unity, the interleaved clock generator means of the first type including a multi-stage serial-delay circuit; and

M interleaved clock generator means of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator means of the first type and for generating in response thereto N/M of the *N* interleaved clock signals, each of the interleaved clock generator means of the second type including a ring counter circuit, wherein:

the input clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes M/2 delay stages, each providing two of the intermediate clock signals.

9. (previously presented) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

interleaved clock generator means of a first type for receiving the input clock signal and for generating in response thereto *M* interleaved intermediate clock signals, where *M* is a factor of *N* and is an integer greater than unity, the interleaved clock generator means of the first type including a ring counter circuit; and

M interleaved clock generator means of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator means of the first type and for generating in response thereto N/M of the *N* interleaved clock signals, each of the interleaved clock signal generator means of the second type including a multi-stage serial-delay circuit.

10. (original) The interleaved clock generator of claim 9, in which the ring counter circuit includes an M-stage ring counter.

11. (original) The interleaved clock generator of claim 9, in which the multi-stage serial-delay circuit includes N/M delay stages, each providing one of the interleaved clock signals.

12. (previously presented) The interleaved clock generator of claim 9, in which:

each intermediate clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes N/2M delay stages, each providing two of the interleaved clock signals.

13. (previously presented) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

an interleaved clock generator of a first type, including a clock input connected to receive the input clock signal, *M* intermediate clock outputs, where *M* is a factor of *N* and is an integer greater than unity, and one of (a) a multi-stage serial-delay circuit and (b) a ring counter circuit, the interleaved clock generator of the first type operating in response to the input clock signal to output a respective intermediate clock signal at each of the intermediate clock outputs; and

M interleaved clock generators of a second type, each including an intermediate clock input connected to a different one of the *M* intermediate clock outputs of the interleaved clock signal generator of the first type, N/M clock outputs and the other of (a) the multi-stage serial-delay circuit and (b) the ring counter circuit, each of the interleaved clock generators of the second type operating in response to the intermediate clock signal to output a respective one of N/M of the interleaved clock signals at each of the clock outputs, wherein:

corresponding edges of temporally adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N*Td);

the input clock signal has a frequency of 1/(M*Td) when the interleaved clock generator of the first type includes the multi-stage serial delay circuit;

the input clock signal has a frequency of M/(N*Td) when the interleaved clock generator of the first type includes the ring counter circuit.

14. (cancel)

15. (original) The interleaved clock generator of claim 13, in which:

the interleaved clock generator of the first type includes the multi-stage serial-delay circuit; and

each of the interleaved clock signal generators of the second type includes the ring counter circuit.

16. (original) The interleaved clock generator of claim 15, in which the ring counter circuit includes an N/M-stage ring counter.

17. (original) The interleaved clock generator of claim 15, in which the multi-stage serial-delay circuit includes M delay stages, each providing one of the intermediate clock signals.

18. (previously presented) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

an interleaved clock generator of a first type, including a clock input connected to receive the input clock signal, *M* intermediate clock outputs, where *M* is a factor of *N* and is an integer greater than unity, and a ring counter circuit, the interleaved clock generator of the first type operating in response to the input clock signal to output a respective intermediate clock signal at each of the intermediate clock outputs; and

M interleaved clock generators of a second type, each including an intermediate clock input connected to a different one of the *M* intermediate clock outputs of the interleaved clock signal generator of the first type, N/M clock outputs and a multi-stage serial-delay circuit, each of the interleaved clock generators of the second type operating in response to the intermediate clock signal to output a respective one of N/M of the interleaved clock signals at each of the clock outputs multi-stage serial-delay circuit.

19. (cancel)

20. (currently amended) The interleaved clock generator of claim ~~19~~,23 in which the ring counter circuit comprises an N/M-stage ring counter.

21. (previously presented) The interleaved clock generator of claim 18, in which:

corresponding edges of temporally-adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N*Td); and

the input clock signal has a frequency of M/(N*Td).

22. (previously presented) The interleaved clock generator of claim 18, in which:

each intermediate clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes N/2M delay stages, each providing two of the interleaved clock signals.

23. (currently amended) ~~The~~ An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising: ~~of claim 19,~~

a multi-stage serial-delay circuit connected to receive the input clock signal, the multi-stage serial-delay circuit including *M* intermediate clock outputs where *M* is a factor of *N* and is an integer greater than unity; and

connected to each of the *M* intermediate clock outputs, a ring counter circuit that generates N/M of the *N* interleaved clock signals, in which:

corresponding edges of temporally-adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N*Td); and

the input clock signal has a frequency of 1/(M*Td).

24. (currently amended) ~~The~~ An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:~~of claim 19,~~

a multi-stage serial-delay circuit connected to receive the input clock signal, the multi-stage serial-delay circuit including *M* intermediate clock outputs where *M* is a factor of *N* and is an integer greater than unity; and

connected to each of the *M* intermediate clock outputs, a ring counter circuit that generates N/M of the *N* interleaved clock signals, in which:

each intermediate clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes M/2 delay stages, each providing two of the intermediate clock signals.

25. (previously presented) An interleaved clock generator for generating *N* interleaved clock signals in response to an input clock signal, where *N* is a non-prime integer, the interleaved clock generator comprising:

a ring counter circuit connected to receive the input clock signal, the ring counter circuit including *M* intermediate clock outputs, where *M* is a factor of *N* and is an integer greater than unity; and

connected to each of the *M* intermediate clock outputs, a multi-stage delay circuit that generates N/M of the *N* interleaved clock signals.

26. (previously presented) The interleaved clock generator of claim 25, in which the ring counter circuit comprises an M-stage ring counter.

27. (previously presented) The interleaved clock generator of claim 25, in which:

corresponding edges of temporally-adjacent ones of the interleaved clock signals differ in time by a time delay Td;

the interleaved clock signals have a frequency of 1/(N*Td); and

the input clock signal has a frequency of M/(N*Td).

28. (previously presented) The interleaved clock generator of claim 25, in which:

each intermediate clock signal comprises differential clock signals each having a 50% duty cycle; and

the multi-stage serial-delay circuit includes N/2M delay stages, each providing two of the interleaved clock signals.